

(use as many sheets as necessary)

Sheet

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First Named Inventor

Takanori SAEKI

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Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		Number	Kind Code ² (if known)		
MT		US 6,184,736	327/295	02-2001	Wissell et al.
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[illegible]

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation ⁶
MT		J. Han et al., "Skew Minimization Techniques for 256M-bit Synchronous DRAM and Beyond", Symposium on VLSI Circuits Digest of Technical Papers (1998), pp. 192-193	
MT		R.B. Watson et al., "Clock Buffer Chip with Absolute Delay Regulation Over Process and Environmental Variations". Proc. of IEEE, Custom Integrated Circuits Conference (1992), pp. 25.2.1-25.2.5	
MT		Y. Okajima, et al., "Digital Delay Locked Loop and Design Technique for High Speed Synchronous Interface", IEICE Trans. Electron, Vol. E79-C, No. 6, June 1996, pp. 798-807	

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